REMARKS

I. Introduction

Claims 1 to 4 are pending. In view of the following remarks, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

Applicants thank the Examiner for considering the Information Disclosure Statement, PTO-1449 papers, and cited references filed April 3, 2008.

II. Rejection of Claims 1 to 4 Under 35 U.S.C. § 102(a)

Claims 1 to 4 were rejected under 35 U.S.C. § 102(a) as anticipated by Cardoso et al., *XPP-VC: A C Compiler with Temporal Partitioning for the PACT-XPP Architecture*, 12th International Conference on Field-Programmable Logic and Applications (FPL) 2002, Proceedings of the Reconfigurable Computing Is Going Mainstream, 2438 Lecture Notes in Computer Science 864-74 (Springer-Verlag) (2002), Berlin, Germany ("the Cardoso reference"). It is respectfully submitted that the Cardoso reference does not anticipate the present claims, and the present rejection should be withdrawn, for the following reasons.

As indicated at http://portal.acm.org/results.cfm?coll=GUIDE&dl=GUIDE&CFID=46254921&CFTOKEN=99672724 (see attached printout of the webpage), the Cardoso reference published in ***September 2002***, which is ***after*** the ***January 18, 2002*** priority date of the present application. In this regard, the present application claims priority to European Patent Application No. 02001331.4, which was filed in English. A claim of priority to European Patent Application No. 02001331.4 was made, *inter alia*, in the Declaration submitted on July 16, 2004, and the Office has acknowledged receipt of all copies of the certified copies of the priority document. In view of the foregoing, it is respectfully submitted that the Cardoso reference does not constitute prior art against the present application.

Withdrawal of this anticipation rejection of claim 1 to 4 is therefore respectfully requested.

III. Conclusion

It is respectfully submitted that all of the presently pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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presents a mapping methodology for coarse-grain reconfigurable arrays which alleviate bandwidth bottleneck by exploiting the processing elements interconnection ...

Keywords: coarse-grain reconfigurable array, data bandwidth optimization, mapping, parallelism, reconfigurable embedded systems, scheduling

9 XPP-VC: A C Compiler with Temporal Partitioning for the PACT-XPP Architecture

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